CLAIMS

What is claimed is:

1. A multi-channel integrator comprising:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output.

2. A multi-channel numerically controlled oscillator comprising the integrator of Claim 1.

3. The multi-channel numerically controlled oscillator of Claim 2 further comprising:

a phase incrementer input multiplexer connected to the integrator input; and

a sine/cosine generation unit connected to the integrator output.

4. The multi-channel numerically controlled oscillator of Claim 2 wherein the numerically controlled oscillator is an M channel numerically controlled oscillator and further wherein the delay section of the integrator comprises at least M delay elements in series.

5. An M channel decimator, wherein M>1, the decimator comprising:

the integrator of Claim 1 wherein the plurality of delay elements comprises at least M delay elements.

6. The M channel decimator of Claim 5 further comprising:

a down-sampler having a down-sampler input connected to the integrator output and a down-sampler output; and

a differentiator connected to the down-sampler output.

7. An N stage multi-channel decimator wherein the decimator comprises an integrator section comprising at least N instances of the integrator of Claim 1 in series.

8. The N stage multi-channel decimator of Claim 7 wherein the decimator is an M channel decimator and further wherein the plurality of delay elements in each integrator comprises at least M delay elements.

9. An M channel interpolator, wherein M>1, the interpolator comprising:

the integrator of Claim 1 wherein the plurality of delay elements comprises at least M delay elements.

10. The M channel interpolator of Claim 9 further comprising:

an up-sampler having an up-sampler output connected to the integrator input and an up-sampler input; and

a differentiator connected to the up-sampler input.

11. An N stage multi-channel interpolator wherein the interpolator comprises an integrator section comprising at least N instances of the integrator of Claim 1 in series.

12. The N stage multi-channel interpolator of Claim 11 wherein the interpolator is an M channel interpolator and further wherein each integrator in the integrator section comprises the integrator of Claim 1 and further wherein the plurality of delay elements comprises at least M delay elements.

13. The integrator of Claim 1 wherein the integrator is implemented in a programmable device.

14. The integrator of Claim 1 wherein the delay section is implemented in one or more embedded memory blocks in a programmable device.

15. A multi-channel differentiator comprising:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output.

16. An M channel decimator, wherein M>1, the decimator comprising:

the differentiator of Claim 15 wherein the plurality of delay elements comprises at least M delay elements.

17. The M channel decimator of Claim 16 further comprising:

a down-sampler having a down-sampler output connected to the differentiator input and a down-sampler input; and

an integrator connected to the down-sampler input.

18. An N stage multi-channel decimator wherein the decimator comprises a differentiator section comprising at least N instances of the differentiator of Claim 15 in series.

19. The N stage multi-channel decimator of Claim 18 wherein the decimator is an M channel decimator and further wherein the plurality of delay elements in each differentiator comprises at least M delay elements.

20. An M channel interpolator, wherein M>1, the interpolator comprising:

the differentiator of Claim 15 wherein the plurality of delay elements comprises at least M delay elements.

21. The M channel interpolator of Claim 20 further comprising:

an up-sampler having an up-sampler input connected to the differentiator output and an up-sampler output; and

an integrator connected to the up-sampler output.

22. An N stage multi-channel interpolator wherein the interpolator comprises a differentiator section comprising at least N instances of the differentiator of Claim 15 in series.

23. The N stage multi-channel interpolator of Claim 22 wherein the interpolator is an M channel interpolator and further wherein the plurality of delay elements in each differentiator comprises at least M delay elements.

24. The differentiator of Claim 15 wherein the integrator is implemented in a programmable device.

25. The differentiator of Claim 15 wherein the delay section is implemented in one or more embedded memory blocks in a programmable device.

26. An N stage, M channel decimator, where M>1, the decimator comprising:

an integrator section comprising:

an integrator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

an integrator section output; and

N integrators connected in series between the integrator section input and the integrator output, wherein each integrator comprises:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output;

a differentiator section comprising:

a differentiator section input;

a differentiator output; and

N differentiators connected in series between the differentiator input and the differentiator output, wherein each differentiator comprises:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output; and

a down-sampler comprising a down-sampler input connected to the integrator section output and a down-sampler output connected to the differentiator section input.

27. An N stage, M channel interpolator, where M>1, the interpolator comprising:

a differentiator section comprising:

a differentiator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

a differentiator output; and

N differentiators connected in series between the differentiator input and the differentiator output, wherein each differentiator comprises:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output;

an integrator section comprising:

an integrator section input;

an integrator section output; and

N integrators connected in series between the integrator section input and the integrator output, wherein each integrator comprises:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output; and

an up-sampler comprising an up-sampler input connected to the differentiator section output and an up-sampler output connected to the integrator section input.

28. An M channel numerically controlled oscillator, where M>1, the numerically controlled oscillator comprising:

an oscillator input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

a sine/cosine generator having a generator input; and

an integrator comprising:

an integrator input connected to the multiplexer output;

an integrator output connected to the generator input;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output.

29. A computer program product for performing multi-channel integration, the computer program product comprising:

a computer usable medium having computer readable code embodied therein, the computer readable code comprising:

computer code for programming a device to create a programmed device, wherein the programmed device comprises:

a multi-channel integrator comprising:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output.

30. A computer program product for performing multi-channel differentiation, the computer program product comprising:

a computer usable medium having computer readable code embodied therein, the computer readable code comprising:

computer code for programming a device to create a programmed device, wherein the programmed device comprises:

a multi-channel differentiator comprising multi-channel differentiator comprising:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output.